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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/265, 21/336, 29/08	A1	(11) International Publication Number: WO 97/42652
		(43) International Publication Date: 13 November 1997 (13.11.97)

(21) International Application Number: PCT/US97/05894

(22) International Filing Date: 11 April 1997 (11.04.97)

(30) Priority Data:
08/647,081 8 May 1996 (08.05.96) US

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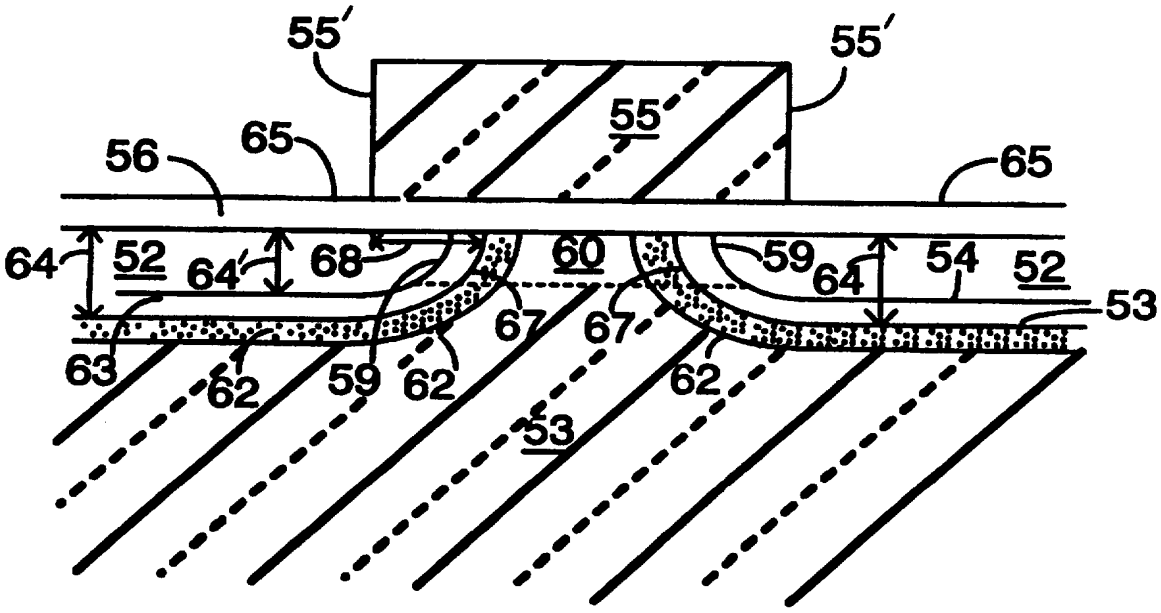
(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: CONTROL OF JUNCTION DEPTH AND CHANNEL LENGTH USING GENERATED INTERSTITIAL GRADIENTS TO OPPOSE DOPANT DIFFUSION



(57) Abstract

An improved manufacturing process and an improved device made by the process for retarding diffusion of implanted dopants during subsequent high-temperature processing. A layer of an electrically inactive species (62) is implanted well below the active dopant layers (52, 70), and the excess interstitials due to damage from the electrically inactive species layer form a retarding gradient which opposes dopant diffusion. Using this process, shallow source-drain junctions (76) can be achieved, and lateral encroachment of LDD implants (52) under the gate (55) can be minimized.

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CONTROL OF JUNCTION DEPTH AND CHANNEL LENGTH USING GENERATED INTERSTITIAL GRADIENTS TO OPPOSE DOPANT DIFFUSION

Technical Field

This invention relates to processes for the formation of shallow implanted regions, and for inhibition of dopant diffusion in integrated circuits.

Background Art

As integrated circuits become smaller and faster, MOS device structures have evolved to necessitate increasingly short channels and shallow junction depths. This presents challenges in the processing of these structures, including ion implantation of dopants to form source, drain, and Lightly Doped Drain (LDD) regions.

Ions are implanted by directing them in a high-energy beam at a target. The ions penetrate a distance into the target, the distance being determined by factors such as ion mass, ion energy, target material and target orientation. The ions are decelerated within the target by a series of collisions or scattering events of two types: collisions with or scattering from the core electrons and nuclei of the target material, and Coulombic interactions with the outer electrons of the target material. If the energy of the ion at any point along its trajectory in the target is given by E, the energy loss due to nuclear collisions is characterized by an energy loss per unit length, $S_n(E)$, called nuclear stopping. The energy loss from interactions with target outer electrons is characterized by an energy loss per unit length $S_e(E)$, called electronic stopping. The total rate of energy loss per unit length is given by the sum of $S_n(E)$ and $S_e(E)$.

A widely used scattering model for calculating nuclear stopping power $S_n(E)$, utilizes a modified Thomas-Fermi screened atomic scattering potential. Based on this model, nuclear stopping increases linearly at low energies, reaches a maximum at some intermediate energy, and decreases at high energies. Nuclear stopping increases with the mass of the implanted ion. The electronic stopping due to inelastic scattering from target outer electrons behaves similarly to stopping of a projectile in a viscous medium, and is approximately proportional to $E^{1/2}$ in the form $S_e(E) \approx k_e E^{1/2}$, with k_e being a constant which is weakly dependent on the ion and target materials.

At low ion energies, nuclear stopping dominates, and there is a threshold energy above which electronic scattering becomes dominant. This crossover energy is dependent on ion mass, being higher for heavier ions. By way of example, for boron, $S_e(E)$ is the predominant energy loss mechanism for ion energies greater than approximately 10keV.

The theoretical distribution of implanted ions would be Gaussian in shape, having a peak at a depth called the projected range R_p. Actual distributions deviate from the ideal, due to channeling effects which occur during implantation, and post implant dopant diffusion.

Channeling during implantation occurs when the high energy ions travel in a single-crystal substrate in directions corresponding to channels. Channels in a single-crystal lattice are aligned in directions along which the ions do not encounter any target nuclei. The ions are channeled or steered along such open channels of the lattice. Those implanted ions that travel down channels are slowed mainly by electronic stopping, and therefore can penetrate the lattice more deeply than can non-channeled ions. Channeling is extremely sensitive to incident

beam direction relative to the lattice in the target. It is difficult to control, and tends to cause anomalous implant profile tails.

Implantation is generally followed by heat treatment to electrically "activate" the implanted ions, which gives the substrate the acceptor or donor behavior. This heat treatment, along with other heat treatments in subsequent processing, also causes diffusion of the implanted ions, which has adverse effects such as increasing the junction depth for source/drain implants, thereby degrading device performance. Diffusion rates vary for the typically used dopants, boron, arsenic, and phosphorus, with boron having the highest diffusion rate. Therefore, diffusion effects are greatest in those PMOS devices which utilize acceptor boron atoms as p-type dopants.

Much effort has been devoted to finding methods of inhibiting undesired positioning and change of positioning of dopants such as boron, during implantation and during post-implant MOS device processing. Many of these methods of inhibiting positional changes utilize the effects of damage associated with implantation. The effective employment of implant-induced damage requires understanding of damage profiles and the physics of damage creation.

Nuclear collisions between energetic implanted ions and the target can cause damage to the target. For a single crystal silicon target substrate, this damage generally consists of displacing silicon atoms from their crystalline lattice sites. In order for a displacement event to occur, the energy transferred to the silicon atom from the collision must be greater than E_{di}, the energy required to displace it from its lattice site. For Si, this value of $E_{di}(Si) \approx 15eV$. A displacement event in Si may yield a vacancy, an unoccupied lattice site. The vacancy may be accompanied by a Si atom occupying a place between lattice sites, called an interstitial Si atom. This vacancy-interstitial Si atom pair forms a point defect known as a Frenkel pair. The implanted ions create zones of gross disorder populated by defects in the regions where they deposit their kinetic energy. The lattice may exhibit several degrees of damage: a) isolated point defects or defect clusters in essentially crystalline silicon; b) local amorphous zones in an otherwise crystalline layer; or c) complete amorphization. An amorphous region is defined as a region lacking crystalline periodicity, and may be described as a region in which the density of displaced atoms per unit volume approaches the atomic density of the semiconductor.

When only electronic scattering events occur, there is insufficient energy transfer to the Si atoms to cause displacement, so that widespread damage does not begin to occur until the ion energy has decreased to the point where nuclear stopping becomes significant. As the ion energy further decreases to below E_{di}, displacement damage ceases. Thus, the highly damaged region in the Si is positioned somewhat shallower than the dopant-implanted region. A graphical representation of damage density profiles as compared with corresponding dopant distribution is shown in Fig. 2, as more fully described hereinafter.

Diffusion of dopant ions through a crystalline silicon lattice follows the basic differential equations of diffusion. If there is an impurity concentration gradient present, dC/dx, in a finite volume of a matrix substance, there will be a tendency for the impurity material to move so that the gradient decreases. If the flow persists for a sufficiently long time, the material will become homogeneous and the net flow of matter will cease. Fick's first law states that

$J = -D[dC(x,t)]/dx$, where

J is the flux of matter across a given plane, and D is the diffusion constant for the material that is diffusing in the specific host medium at a specific temperature. If Fick's first law is modified to include a concentration gradient decreasing with time, and assuming a thin layer of dopant as an initial condition, the concentration of dopants after thermal anneal at a specific temperature for a period of time is approximated by a Gaussian distribution.

The ions boron, arsenic, phosphorus, and antimony which are used as dopants in integrated circuit manufacturing, are all substitutional impurities, which situate themselves at lattice points in the silicon lattice. Recent models indicate that for many species of ions, diffusion between vacancies in the lattice is controlled both by the vacancy concentration and by the concentration of silicon interstitials, i.e., those Si atoms displaced from their lattice sites. These diffusion mechanisms occur in single crystal silicon. They are to be distinguished from different diffusion mechanisms which occur in polysilicon or amorphous silicon. In the single crystal case, the diffusion constant D of the substitutional impurity can be expressed as

$D = D_I + D_V$, where D_I and D_V are the interstitial and vacancy components of the diffusion coefficient. The relative values of D_I and D_V vary for different ions: The dopants boron, indium and phosphorus are believed to diffuse primarily via interstitial or interstitialcy mechanisms as shown in Fig. 3, which are described by S. Crowder in his *Ph.D. dissertation, Stanford University, 1995, pp 41-43.* The diffusivities of these dopants are therefore controlled mostly by Si interstitial concentration. Antimony diffusion is primarily vacancy-controlled, due to its large size which physically prohibits the ions from moving through the interstitial spaces. It therefore diffuses via the slow process of jumping from one vacancy to an adjacent vacancy. Some ions such as arsenic can move by both interstitial and vacancy mechanisms. Whereas vacancies are caused almost exclusively by the creation of point defects during implantation, silicon interstitials can also be caused by a kick-out effect upon commencement of annealing. In this case, a dopant ion kicks out one Si atom to become a substitutional, and the silicon atom becomes an excess interstitial. A model of interstitial profiles based on this mechanism, known as the +1 model, is described by M. Giles in *J. Electrochem Soc, 138, 1160 (1991).*

The presence of excess silicon interstitials in the vicinity of an implanted dopant distribution such as boron causes an effect known as Transient Enhanced Diffusion (TED). This effect is characterized by a gradient in the concentration profile of excess interstitials causing a large enhancement in dopant diffusion rate in the "downhill" direction of the negative gradient. This effect is short in duration, lasting only several minutes at temperatures as low as 800°C, and only seconds at higher temperatures, until the excess interstitials recombine or are otherwise removed from the vicinity of the dopant. However, during this short period, effective diffusivity of dopants can be enhanced by a factor of more than 10,000. Since the damage peak is positioned slightly shallower than the dopant peak, the enhanced diffusion tends to shift the dopants deeper into the silicon. As a result, the motion of the dopant atoms due to the damage created by the implant process is a primary determining factor of the final junction depths and profile shapes.

Intentional creation of damaged regions by implantation of electrically inactive species has been utilized to inhibit undesired positioning or motion of dopants. Kase et al, in *U.S. Patent #5,145,794 (1992)* describe a method of inhibiting channeling during implantation. According to this method, argon is pre-implanted to create a partially crystalline disordered silicon layer, and thereafter boron is implanted directly into the disordered

region. Using this method, boron channeling is largely avoided. The silicon damage can be repaired by subsequent anneal.

Similar methods have been proposed to inhibit dopant diffusion during post-implant anneal. Milgram et al, in *Appl. Phy. Lett. 42, 878 (1983)*, describe pre-implantation of an argon dose which is sufficient to produce an amorphous layer, followed by implantation of boron into the amorphous region. The implanted argon causes a decrease in the diffusion of boron in the silicon during post-implant anneals up to temperatures of 900°C. The authors conclude that the boron atoms are trapped by the incorporated argon atoms. It is known that inhibition of dopant diffusion by creation of an amorphous layer causes problems because the defects induced thereby in the silicon crystal are not completely eliminated by a later annealing, but are partially retained, degrading the semiconductor device characteristics. Methods of inhibiting dopant diffusion in single-crystal silicon without causing amorphization are therefore needed.

Disclosure of Invention

I have provided a process for utilizing implant damage-induced interstitial gradients to inhibit dopant diffusion in crystalline silicon, thereby retaining shallow implanted junctions, and retarding lateral spreading of dopants under the gate of an MOS structure.

According to my invention, an integrated circuit process and a product formed utilizing this process is provided for retarding subsequent diffusion of a region of implanted dopant atoms in crystalline silicon, whereby an electrically inactive species is implanted well below the dopant implant

An aspect of this invention is an improved process for providing shallow source/drain junctions for MOS devices.

Another aspect of this invention is a process for retarding diffusion of dopant atoms implanted into crystalline silicon during subsequent high temperature processing cycles.

A further aspect is a process for retarding subsequent diffusion of a region of implanted dopant atoms in crystalline silicon which does not cause formation of an amorphous layer in the silicon.

A further aspect of this invention is to a process for forming implanted Lightly Doped Drain (LDD) structures in MOS devices which retards lateral spread of the LDD region under the gate.

A further aspect of this invention is an MOS device formed using this process and having shallow source/drain junction and having lowered lateral diffusion of LDD implant under the gate.

Brief Description of the Drawings

Figure 1 is a graph of implanted boron profiles in single crystal silicon after anneal at various temperatures.

Figure 2 is a graph of calculated damage profiles resulting from boron implantation at various energies.

Figure 3 is a schematic representation of boron diffusion mechanisms.

Figure 4 is a graphical representation of implanted ion profiles and damage profiles for a double implant utilizing this invention.

Figure 5 is a process flow for a preferred embodiment of this invention.

Figure 6a is a schematic cross sectional view of a prior art MOS structure having LDD implants.

Figure 6b is a schematic cross sectional view of an MOS structure having LDD implants and a retarding

implant utilizing this invention.

Figure 7 is a cross sectional view of an MOS structure having LDD and source/drain implants and retarding implants of varying energies.

Modes for Carrying out the Invention

According to this invention, in an integrated circuit manufacturing process employing ion implantation to dope a semiconductor, an electrically inactive species is implanted well beneath the dopant implant to retard diffusion of the implant deeper into the semiconductor.

Figure 1 shows a typical,well known, as-implanted profile of boron dopant atoms in single crystal silicon, along with profiles after 35 minute furnace anneals at temperatures ranging between 700°C and 1100°C. The diffusion occurring during the anneal cycles broadens the dopant profiles and shifts the leading edge deeper into the substrate, causing the aforementioned problems in MOS device performance.

Figure 2 shows well known calculated damage density profiles caused by boron implantation at energies ranging between 10 KeV and 1000 KeV. The depth X into the sample is normalized by the projected range R_p of the implanted ions themselves. The calculated damage density profiles are similar in shape to the ideal as-implanted boron profile, but the peak position is at a shallower depth than the dopant peak position. At higher implant energies the damage peak more closely coincides with the dopant peak.

Figure 3 shows a model of the motion of dopants through a silicon lattice via interstitial, interstitialcy, and vacancy mechanisms. In interstitial kickout, a substitutional dopant atom 2 in a lattice site of silicon lattice 4 is "kicked out" by a silicon interstitial atom 6, after which dopant atom 2 moves between lattice sites 8 through interstitial region 10 until it encounters another vacant site or itself kicks out an atom from an occupied site. The interstitialcy mechanism schematic shows a silicon interstitial atom 12 doubly occupying silicon lattice site 14 along with silicon atom 15. Interstitial 12 then moves to doubly occupy lattice site 16 along with dopant atom 18, which then moves to doubly occupy lattice site 20 with silicon atom 22. These interstitial and interstitialcy mechanisms, which are the dominant diffusion mechanisms for boron, indium, and phosphorus, provide for much faster diffusion rate than does the vacancy mechanism, whereby dopant atom 24 moves only from lattice site 26 to neighboring vacancy 28, leaving vacancy 29.

With reference to Figure 4, a concentration profile is shown for a double implant structure utilizing this inventive process. The structure comprises a dopant species, boron by way of example, having concentration peak 30 at depth d_1, and an electrically inactive species, argon by way of example, having concentration peak 32 at depth d_2, well below d_1. Damage from implantation of the dopant species results in silicon interstitial peak 34 at depth d_3, slightly shallower than depth d_1 of dopant peak 30. Similarly, damage from implantation of the electrically non-active species results in silicon interstitial peak 36 at depth d_4, slightly shallower than depth d_2 of peak 32, but deeper than depth d_1 of dopant peak 30. Interstitial gradient 38, which is negative towards greater depth, is associated with interstitial peak 34 and causes transient enhanced diffusion of the dopant into the silicon during subsequent anneal. This would increase junction depth if the dopant implant were a source/drain or LDD implant. However, the negative or "downhill" direction of interstitial gradient 40 associated with interstitial peak 36 from the electrically inactive species implant, is towards the surface. Gradient 40 would thereby oppose

diffusion of the dopant deeper into the silicon during subsequent anneal. Gradient 38 is termed the "accelerating gradient", and gradient 40 is termed the "retarding gradient". To achieve the retarding effect, peak 32 is positioned sufficiently deeper than dopant peak 30 so that interstitial gradient 40 is deeper than the dopant atoms to be retarded. Implantation of the electrically inactive species, thereby forming a "retarding implant", may precede or follow implantation of the dopant species.

With reference to Figure 5, a process flow is shown for a preferred embodiment of my invention as it would be applied to the source/drain and LDD implants of a PMOS transistor with a polysilicon gate, as illustrated in Fig. 7. In Step 42, a silicon substrate is provided having a grown gate oxide at its surface and having a polysilicon gate thereon. In Step 44, implantation of boron LDD structures is performed, using standard methods with the polysilicon gate serving as an implant mask, and the implanted dopant species ions penetrating the substrate in the regions not covered by the polysilicon. Typical doses for Step 44 implant are 4-5 E13/cm^2, energies of 25-35 KeV using BF_2^+ ions as the implanted boron-containing species. In Step 46, a further implantation is performed, this time with argon at a 1 E13 to 1 E14 dose range, with the polysilicon gate serving as the implant mask, and with the implantation energy, which is generally in the 300-400 KeV range, selected so that the resulting non-active argon concentration peak is positioned well below the LDD implant (Fig. 6b, 62). In Step 48, gate sidewall spacers of 1000-1500 Angstroms width are generally formed using standard deposition and etchback techniques (Fig. 7, 72). Sidewall spacers are not always required, so this step may be optional. In Step 50, implantation of source/drain structures is performed, using standard methods, with the polysilicon gate (and sidewall spacers) serving as an implant mask. Typical source/drain implantation parameters are in the ranges of 50-100 KeV energy, 1 E15 to 5 E15 dose. Standard Rapid Thermal Anneal steps may be implemented during the process. These are typically in the range of 980-1050°C for 30 to 60 seconds.

With reference to prior art Figure 6a, LDD regions with implants 52 of boron, by way of example, are shown in silicon substrate 53 having surface 51, with junction 54,59 therebetween. Polysilicon gate 55 with edges 55'is over gate oxide 56 and serves as a mask for implants 52. The implanted ions penetrate into the substrate through regions 57 not covered by polysilicon 55. Side scatter during implantation causes LDD implants to extend laterally beneath gate 55 a lateral distance 58, to lateral junction portion 59. The vertically displaced junction portion 54 at depth 64' and lateral junction portion 59 together comprise the "leading edge" of the LDD implant. Channel 60 is disposed between implants 52. Without utilizing my invention, annealing results in diffusion of implants 52 and causes motion of the dopant atoms in the direction of arrows 61, causing junction portion 54 to deepen and channel 60 to shorten.

With reference to Figure 6b, according to my invention, additional retarding implants 62 of an electrically inactive species, argon by way of example, are positioned with trailing edge portions 63 forming a boundary portion between the inactive implant 62 and the substrate 53, at a vertical depth 64 well below depth 64' of LDD implant junctions 54. Polysilicon gate 55 serves as a mask for retarding implants 62, the implanted ions penetrating into the substrate through regions 65 not covered by polysilicon 55. Side scatter causes lateral trailing edge portions 67 of implants 62 to extend a lateral distance 68 beneath gate 55 which is greater than the lateral distance 58 of edges 59 of the LDD active species implant, edge portion 67 thereby forming a second boundary

portion. In this case, dopant and damage profiles in the lateral direction are equivalent to those extending vertically into the substrate, as previously described. Therefore, the presence of the retarding implants further beneath the gate both impedes lateral diffusion of LDD active species implants into channel region 60, thereby decreasing short-channel effects for a given gate dimension, and also impedes vertical diffusion of the active species into the substrate.

With reference to Figure 7, showing LDD region 52, sidewall spacer 72, and source/drain structures, the LDD implant 52 extends under gate 55 a distance 58' to junction portion 59. Source/drain implant 70 is masked by polysilicon gate 55 and by sidewall spacer 72, and extends laterally to form junction portion 74. Source/drain vertically displaced junction portion 76 is deeper than LDD junction portion 54, but source/drain lateral junction portion 74 does not extend as far under gate 55 as does LDD lateral junction portion 59. Electrically inactive retarding implants 78, 62, having different implantation energies are shown. Lower energy implant 78 extends deeper than both source/drain junction 76 and LDD junction 54. However, its lateral edge 80 is between junction 59 of LDD implant and junction 74 of source/drain implant. Therefore, while implant 78 would retard lateral diffusion of source/drain implant 70, it would enhance and accelerate lateral spread of LDD implant 52. Higher energy retarding implant 62 is positioned deeper (63) than both source/drain junction 76 and LDD junction 54. Additionally, its lateral edge 67 extends further beneath gate 55 than do junction 59 of LDD implant and junction 74 of source/drain implant. Implant 62 would retard both vertical and lateral diffusion of LDD and source/drain implants. Optimum energy of the retarding implant depends on LDD implant energy and dose, source/drain energy and dose, width of sidewall spacer, and temperature and duration of post-implant heat cycles. By way of example, for a case where the LDD spacer oxide width is approx. 1300 Angstroms, the N^+ implant is As^+ implanted @ 80 KeV, the NLDD implant is phosphorous implanted @ 25 KeV and baked at 900°C for approx. 45 minutes, the retarding implant 62 will be implanted at an energy, chosen in the 300-400 KeV range, to reach its R_p (measured laterally under the gate, not vertically) at 3000 Angstroms, with the resultant peak of interstitials at 2400 Angstroms.

Industrial Applicability

Utilizing my invention, diffusion of dopants during high temperature post-anneal processing will be retarded by the opposing interstitial gradient. This effect, while transient in nature, is expected to have large impact on final dopant profiles, since it will occur during the critical period of transient enhanced diffusion caused by the damage from the retarding implant. As a result of my invention, source-drain junctions will diffuse less and therefore remain shallower, and lateral spread of LDD implants into the channel region will be decreased. The process will not cause formation of an amorphous layer because the retarding implant doses are only in the range of 1 E13 to 1 E14, therefore implant damage will be repaired by subsequent anneal steps. The process is easily incorporated into standard MOS manufacturing process flows.

Whereas the invention as described utilizes a boron LDD and source/drain implant and an argon retarding implant following LDD implant, it is not essential that this exact process be followed. By way of example, the retarding implant could be performed before the LDD implant, using the gate as a mask, or it could be performed

after the sidewall spacers were formed, either before or after the source/drain implant. In this case, a higher retarding implant energy would be required to position the lateral edge of the retarding implant further under the gate than the lateral edge of the LDD implant. Also by way of example, this invention would also be effective in retarding arsenic or phosphorus LDD and source/drain implant diffusion. Additionally, the retarding implant could be comprised of any electrically inactive species, preferably of relatively low atomic mass. The scope of the invention should be construed in light of the claims. With this in mind,

I claim:

1. An ion implantation method for reducing positional changes in active dopants during high temperature processing of a semiconductor substrate,(53) wherein said substrate has been provided with a masking pattern on said substrate and said masked substrate has been implanted with a first dose of an active dopant to have a peak dopant concentration (30) at a first depth into said substrate, characterized by:

thereafter bombarding said masked substrate (53) with high energy ions to implant a second dose of an electrically inactive ion species to have a peak concentration (32) at a second depth into said substrate, said second depth being 500-1000 Angstroms greater than said first depth, said second dose being sufficiently low to avoid formation of an amorphous layer in said substrate; and

annealing said substrate.

2. An integrated circuit manufacturing process employing ion implantation for doping crystalline silicon, comprising the steps of:

providing a single crystal silicon substrate (53) having a surface (51) with a masking pattern thereon having first and second pattern surface portions, said first pattern surface portion having an edge (55'), said first and second pattern surface portions having different ion transmission characteristics;

implanting a first dose of active dopant ions at a first ion energy into said substrate through said first surface portion (65) to form a first crystalline implanted region (52) in said substrate, said first crystalline implanted region having a dopant concentration peak of said active dopant therein, said first region further having a first leading edge (54,59) forming a first junction between said first region and said substrate, said first junction having a first junction portion (54) at a first depth (64') below said first surface portion, and a second junction portion (59) which curves back to intersect said surface of said substrate at a first lateral distance (58) measured along said silicon surface from said edge of said first surface pattern portion;

implanting a second dose of an electrically inactive ion species at a second ion energy into said substrate through said first surface portion to form a second crystalline implanted region (62) in said substrate, said second implanted region having an electrically inactive species concentration peak therein, said second implanted region also having a trailing edge (63,67), said trailing edge forming a boundary between said second crystalline implanted region and said substrate, said boundary having a first boundary portion (63) at a second depth (64) below said first surface portion and a second boundary portion (67) which curves back to intersect said surface of said substrate at a second lateral distance(68) measured alond said silicon surface from said edge of said first surface pattern portion, said second depth being larger than said first depth, and said second lateral distance being larger than said first lateral distance; and

heating said crystalline silicon at high enough temperature to activate said active dopant and to anneal crystalline damage, whereby vertical and lateral movement of said active dopant into said crystalline substrate is retarded by said inactive ion species implant.

3. The process of claim 2, wherein:

said concentration peak of said electrically inactive species is at a distance in the range between 500-1000

Angstroms from said dopant concentration peak of said first region;

said dopant ion species is selected from a group consisting of boron, arsenic, and phosphorus; and

said electrically inactive ions are selected from a group consisting of argon, silicon, helium, and germanium.

4. The process of claim 2, wherein the step of providing said silicon substrate includes providing a gate oxide thereon, and wherein said second pattern surface portion comprises a conducting gate above said gate oxide.

5. The process of claim 4, wherein: said concentration peak of said electrically inactive species is at a distance in the range between 500-1000 Angstroms from said dopant concentration peak of said first region;

said dopant ion species is selected from a group consisting of boron, arsenic, and phosphorus;

said electrically inactive ions comprise argon;

said first ion energy is in the range between 25-100 KeV, and said second ion energy is in the range between 100-400 KeV.

6. An integrated circuit MOS manufacturing process for retarding diffusion of implanted dopants during subsequent high-temperature processing, comprising the steps of:

providing a single crystal silicon substrate (53) having a surface (51) with a gate oxide (56) thereon, said surface having a gate electrode (55) with edges (55') thereon, and said surface having a first surface portion (65) not covered by said gate electrode;

implanting a first dose of dopant ions at a first ion energy into said substrate through said first surface portion to form a first crystalline implanted dopant region (53) in said substrate, said first implanted dopant region having a first dopant concentration peak therein, and having a first leading edge (54,59) forming a first junction between said first implanted dopant region and said substrate, said first junction having a first junction portion (54) at a first depth (64') below said first surface portion, and a second junction portion (59) which curves back to intersect said surface of said substrate at a first lateral distance (58) measured along said silicon surface from said edge of said first surface portion;

forming insulating sidewall spacers (72) abutting said gate edges, said spacers having a width (74') and additionally covering a second portion of said surface, said surface having a third portion not covered by said gate or said sidewall spacers;

implanting a second dose of dopant ions at a second ion energy into said substrate through said third surface portion to form a second crystalline implanted dopant region (70) in said substrate, said second implanted dopant region having a second dopant concentration peak therein, and having a second leading edge (74,76) forming a second junction between said second implanted dopant region and said substrate, said second junction having a first junction portion (76) at a second depth (76') below said surface, and a second junction portion (74) which curves back towards and intersects said surface of said silicon substrate after extending under said sidewall spacer a second lateral distance (74') measured along said surface of said substrate, said second lateral distance being less than the sum of said sidewall spacer width and said first lateral distance;

following said step of forming said sidewall spacers, and preceding or following said second dopant implantation step, implanting a third dose of electrically inactive ions at a third ion energy into said substrate through said third surface portion to form a third crystalline implanted region (62) in said substrate, said third

implanted region having an electrically inactive species concentration peak therein, and having a trailing edge (67,63), said trailing edge forming a boundary between said third implanted region and said substrate, said boundary having a first boundary portion at a third depth (64) below said surface of said silicon substrate and a second boundary portion (67) which curves back toward and intersects said surface of said substrate under said gate at a third lateral distance (68) measured along said surface of said substrate from said gate edge, said third depth being larger than both said first depth and said second depth, and said third lateral distance being larger than said first lateral distance.

7. The process of claim 6, wherein:

said concentration peak of said electrically inactive species is at a distance in the range between 500-1000 Angstroms from said dopant concentration peak of said first region;

said dopant ion species is selected from a group consisting of boron, arsenic, and phosphorus;

said electrically inactive ions comprise argon;

said first ion energy is in the range between 10-50 KeV, said first ion dose is in the range between 1E13 to 5E13, said second ion energy is in the range between 50-100 KeV, said second ion dose is in the range between 1E15 to 5E15, said third ion energy is in the range between 300-400 KeV, said third ion dose is in the range between 1E13 to 1E14, and said sidewall spacer width is in the range between 1000-1500 Angstroms.

8. An intermediate integrated circuit product formed adjacent a surface (51) of a silicon substrate (53), said intermediate product comprising:

a gate electrode (55), said gate electrode being mounted above said silicon substrate surface (51); a portion of said silicon substrate surface (51) not beneath said gate electrode being a first surface portion (65), said gate electrode having an edge (55') which also defines the edge of said first surface portion;

a first implanted dopant region (52) in said substrate, said first implanted dopant region having an active dopant concentration peak therein, said first implanted dopant region also having a first leading edge (54, 59) forming a first junction between said first implanted dopant region and said substrate, said first junction having both a first junction portion (54) at a first depth (64') below said first surface portion and a second junction portion (59) which curves back to intersect said surface of said substrate at a first lateral distance (58), measured along said silicon surface from said edge (55') of said first surface portion;

a second crystalline implanted region (62) in said substrate, said second crystalline implanted region having an electrically inactive species concentration peak therein, said second crystalline implanted region having a trailing edge, said trailing edge (63,67) forming a boundary between said second crystalline implanted region (62) and said substrate (53), said boundary having a first boundary portion (63) at a second depth (64) below said first surface portion and a second boundary portion (67) which curves back to intersect said surface of said substrate at a second lateral distance (68) measured along said silicon surface from said edge (55') of said first surface portion, said second depth (64) being larger than said first depth (64'), and said second lateral distance (68) being larger than said first lateral distance (58).

9. The product of claim 8, wherein:

said concentration peak of said electrically inactive species is at a distance in the range between 500-1000

Angstroms from said dopant concentration peak of said first region;

said dopant ion species is selected from a group consisting of boron, arsenic, and phosphorus; and

said electrically inactive ions comprise argon.

10. An intermediate integrated circuit product formed adjacent a surface (51) of a silicon substrate, said product being an MOS structure having a conductive gate, implanted source/drain, and Lightly Doped Drain regions, comprising:

a gate oxide (56) on said surface of said silicon substrate;

a gate electrode (55), said gate electrode being mounted above said silicon substrate surface (51); a portion of said silicon substrate surface (51) not beneath said gate electrode being a first surface portion (65), said gate electrode having an edge (55') which also defines the edge of said first surface portion;

a first implanted dopant region (52) in said substrate, said first implanted dopant region having an active dopant concentration peak therein, said first implanted dopant region also having a first leading edge (54, 59) forming a first junction between said first implanted dopant region and said substrate, said first junction having both a first junction portion (54) at a first depth (64') below said first surface portion and a second junction portion (59) which curves back to intersect said surface of said substrate at a first lateral distance (58), measured along said silicon surface from said edge (55') of said first surface portion;

a sidewall spacer (72), said sidewall spacer abutting said gate edge, said spacer having a width (72') and additionally covering a second portion of said surface of said silicon substrate, said second portion of said surface of said silicon substrate being a portion of said first surface portion of said surface of said silicon substrate;

a second implanted dopant region (70) extending beneath said sidewall spacer, said second implanted dopant region having a second dopant concentration peak therein and having a second leading edge (76, 74) forming a second junction located between said second implanted dopant region and said substrate, said second junction having a first junction portion (76) at a second depth (76') below said surface, and a second junction portion (74) which curves back towards and intersects said surface of said silicon substrate after extending under said sidewall spacer a second lateral distance (74') measured along said single surface of said silicon substrate, said second lateral distance (74') being less than the sum of said sidewall spacer width (72') and said first lateral distance (58);

a third crystalline implanted region (62) including an implanted electrically inactive species beneath said gate and said sidewall spacer, said third crystalline implanted region having an electrically inactive species concentration peak therein, and having a trailing edge (67, 63), said trailing edge forming a boundary between said third crystalline implanted region (62) and said substrate (53), said boundary having a first boundary portion (63) at a third depth (64) below said surface of said silicon substrate and a second boundary portion (67) which curves back toward and intersects said surface of said silicon substrate under said gate at a third lateral distance (68) measured along said surface of said silicon substrate from said gate edge (55'), said third depth (64) being larger than both said first depth (64') and said second depth (76'), and said third lateral distance (68) being larger than said first lateral distance (58).

11. The product of claim 10, wherein:

said concentration peak of said electrically inactive species is at a distance in the range between 500-1000

Angstroms from said dopant concentration peak of said first region;

said dopant ion species is selected from a group consisting of boron, arsenic, and phosphorus; and

said electrically inactive ions comprise argon;

said first ion dose is in the range between 1E13 to 5E13, said second ion said second ion dose is in the range between 1E15 to 5E15, said third ion dose is in the range between 1E13 to 1E14, and said sidewall spacer width is in the range between 1000-1500 Angstroms.

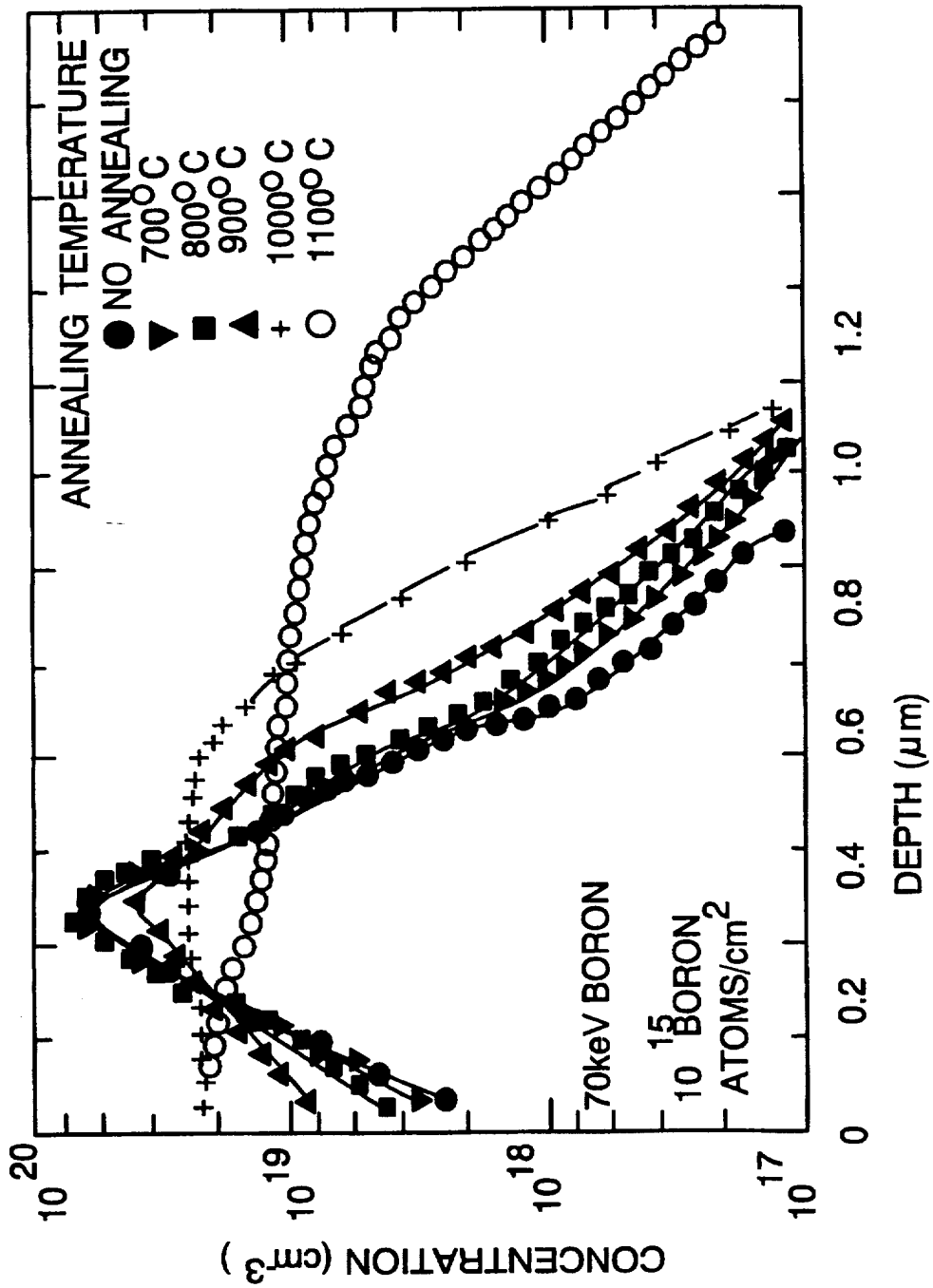
ANNEALING TEMPERATURE
NO ANNEALING
700°C
800°C
900°C
1000°C
1100°C
70keV BORON
10^15 BORON ATOMS/cm^2
CONCENTRATION (cm^-3)
DEPTH (μm)
10^20
10^19
10^18
10^17
0
0.2
0.4
0.6
0.8
1.0
1.2

FIG. 1

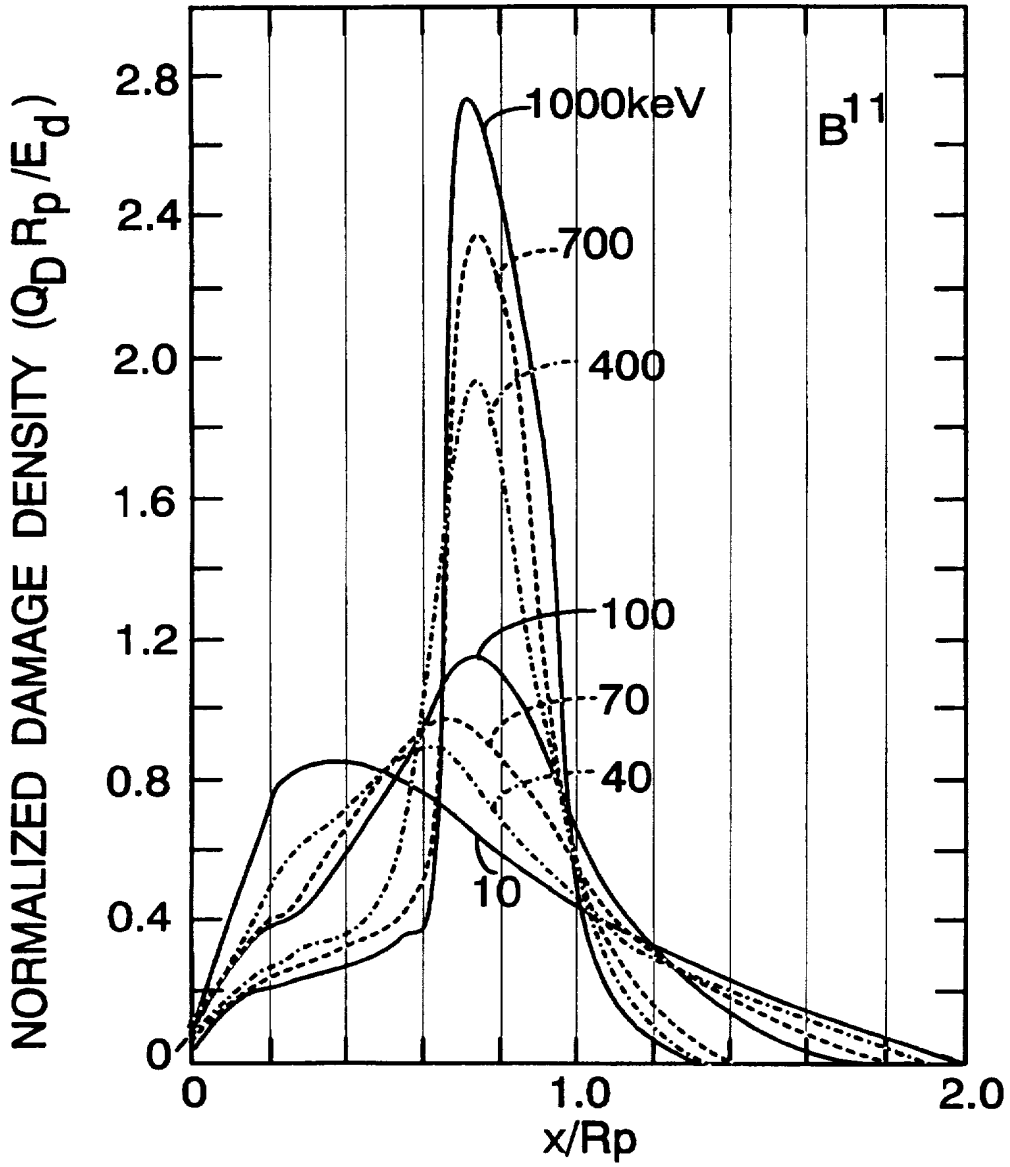
NORMALIZED DAMAGE DENSITY ($Q_D R_p/E_d$)
2.8
2.4
2.0
1.6
1.2
0.8
0.4
0
0
1.0
2.0
x/Rp
1000keV
700
400
100
70
40
10
B^{11}

FIG. 2

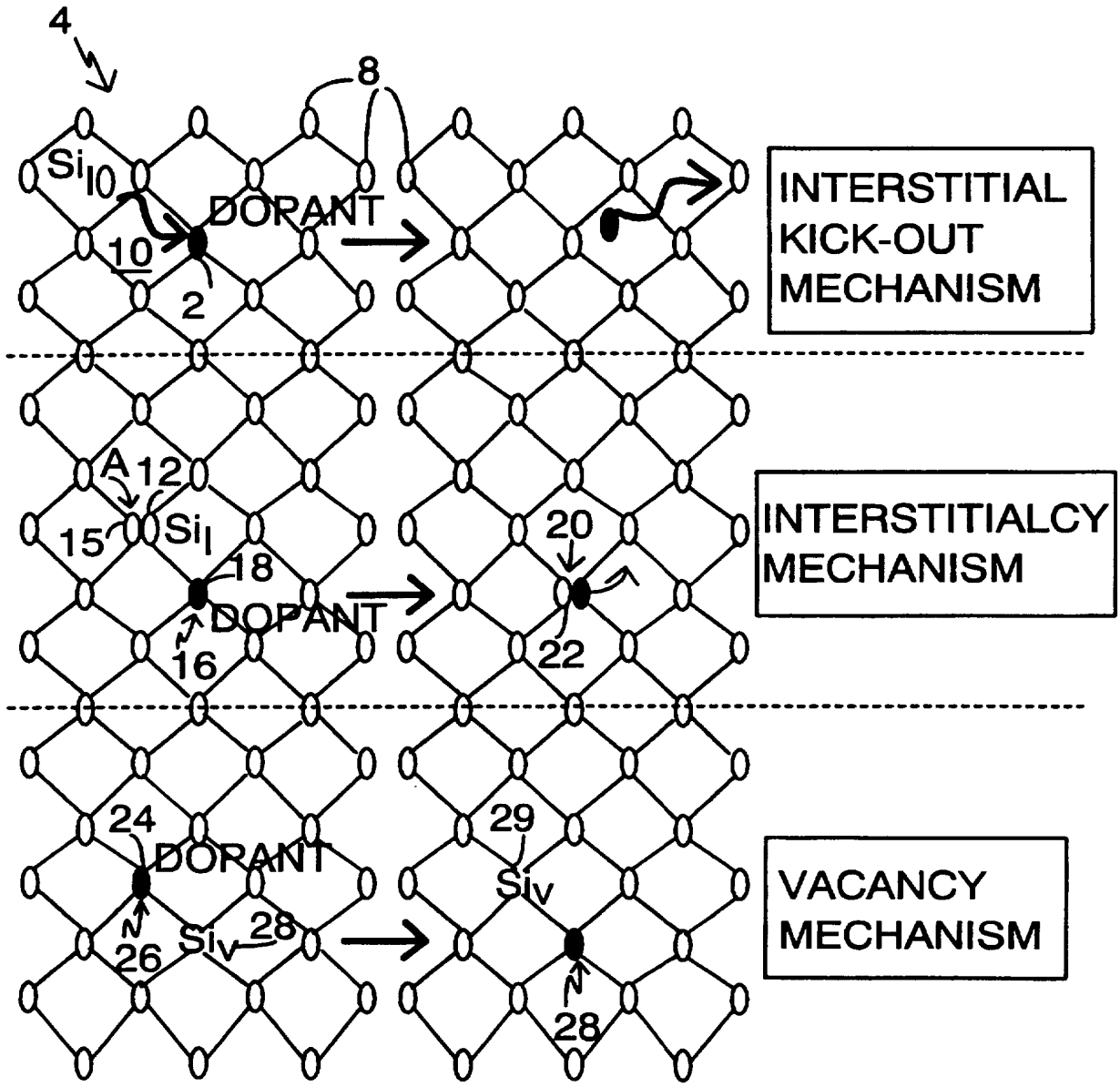
4
8
Si_{I0}
DOPANT
10
2
INTERSTITIAL KICK-OUT MECHANISM
A
12
15
Si_I
18
DOPANT
16
20
22
INTERSTITIALCY MECHANISM
24
DOPANT
26
Si_V
28
29
Si_V
28
VACANCY MECHANISM

FIG. 3

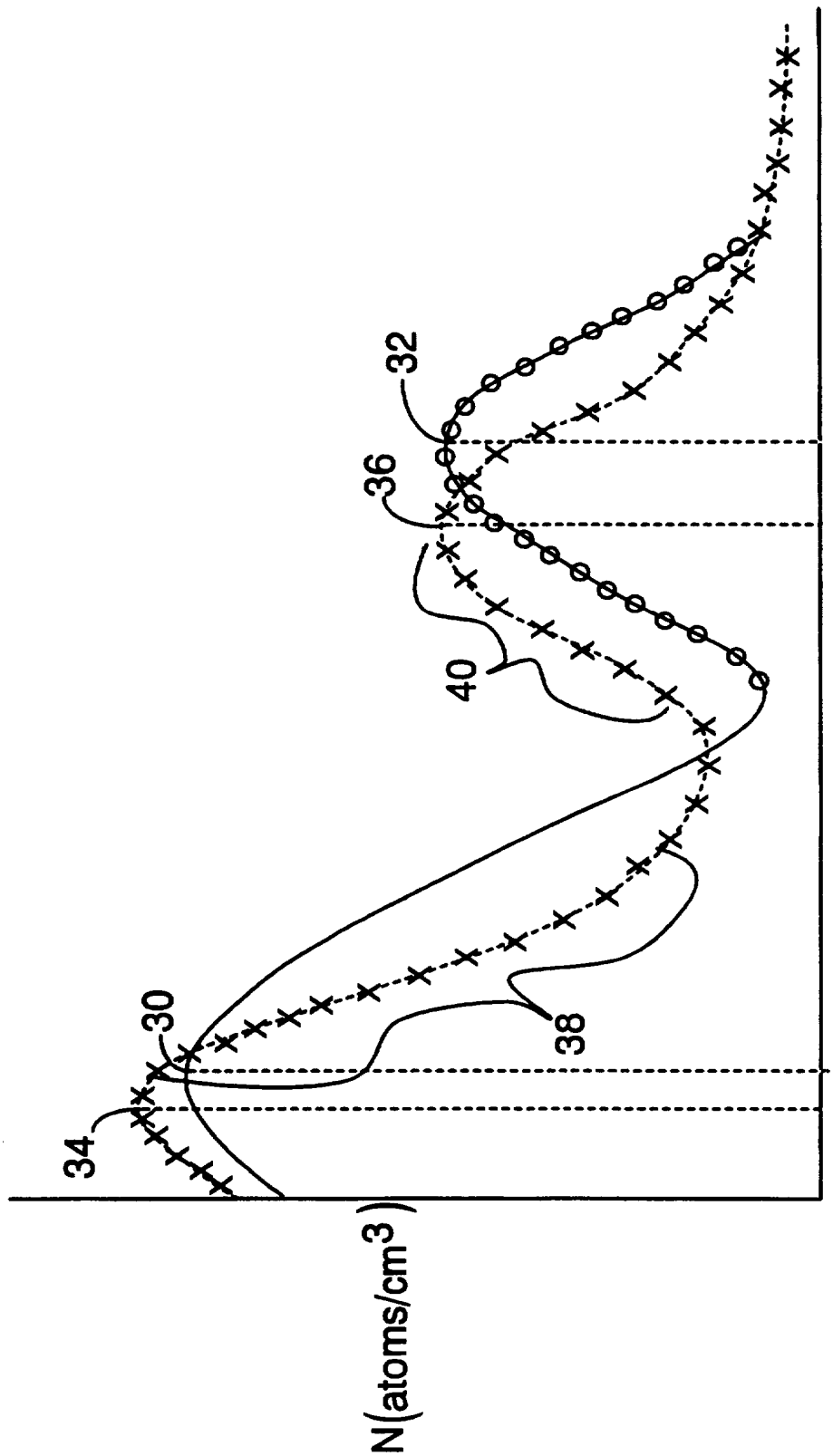

FIG. 4

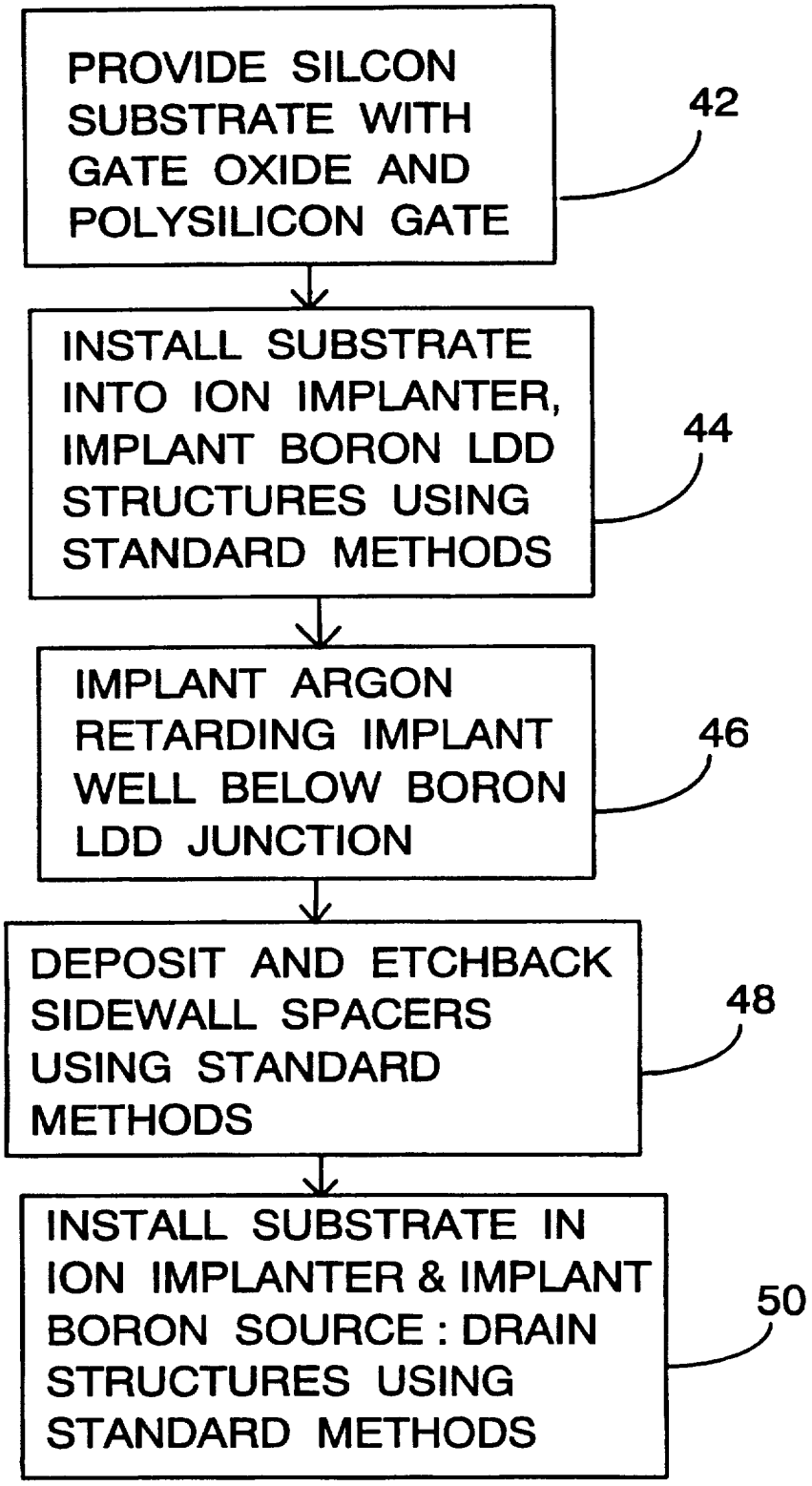
PROVIDE SILCON SUBSTRATE WITH GATE OXIDE AND POLYSILICON GATE
42
INSTALL SUBSTRATE INTO ION IMPLANTER, IMPLANT BORON LDD STRUCTURES USING STANDARD METHODS
44
IMPLANT ARGON RETARDING IMPLANT WELL BELOW BORON LDD JUNCTION
46
DEPOSIT AND ETCHBACK SIDEWALL SPACERS USING STANDARD METHODS
48
INSTALL SUBSTRATE IN ION IMPLANTER & IMPLANT BORON SOURCE : DRAIN STRUCTURES USING STANDARD METHODS
50

FIG. 5

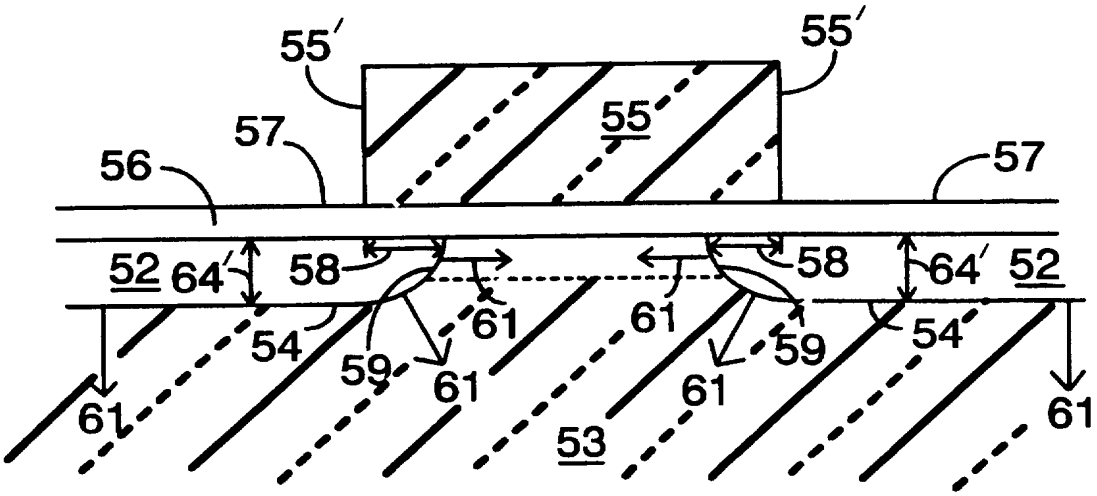

FIG. 6A
PRIOR ART

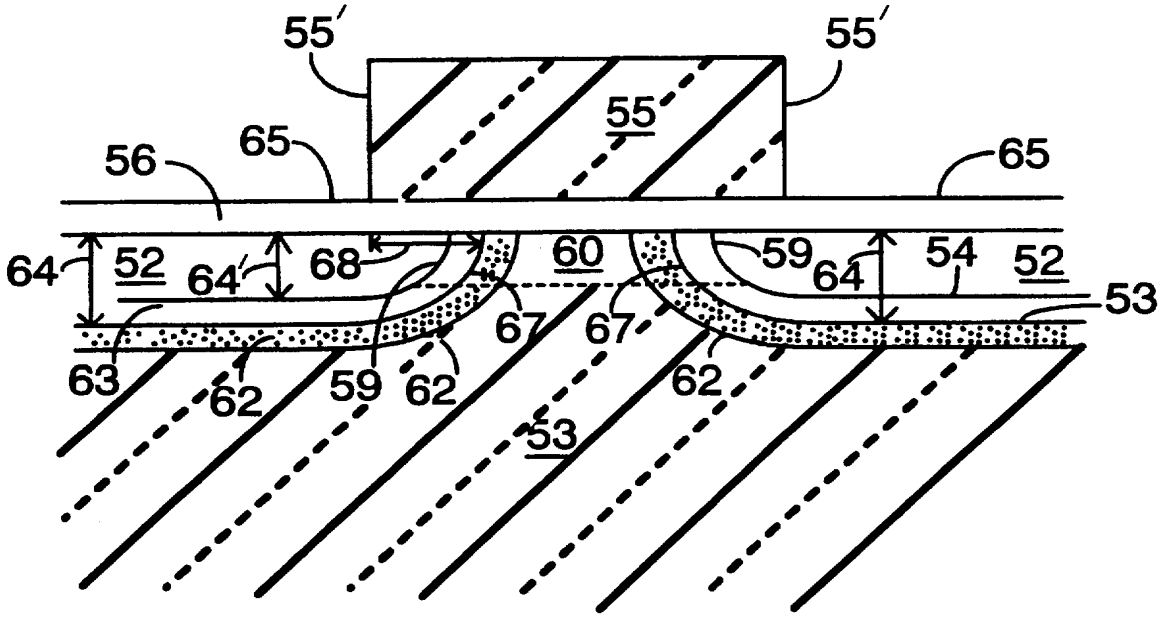

FIG. 6B

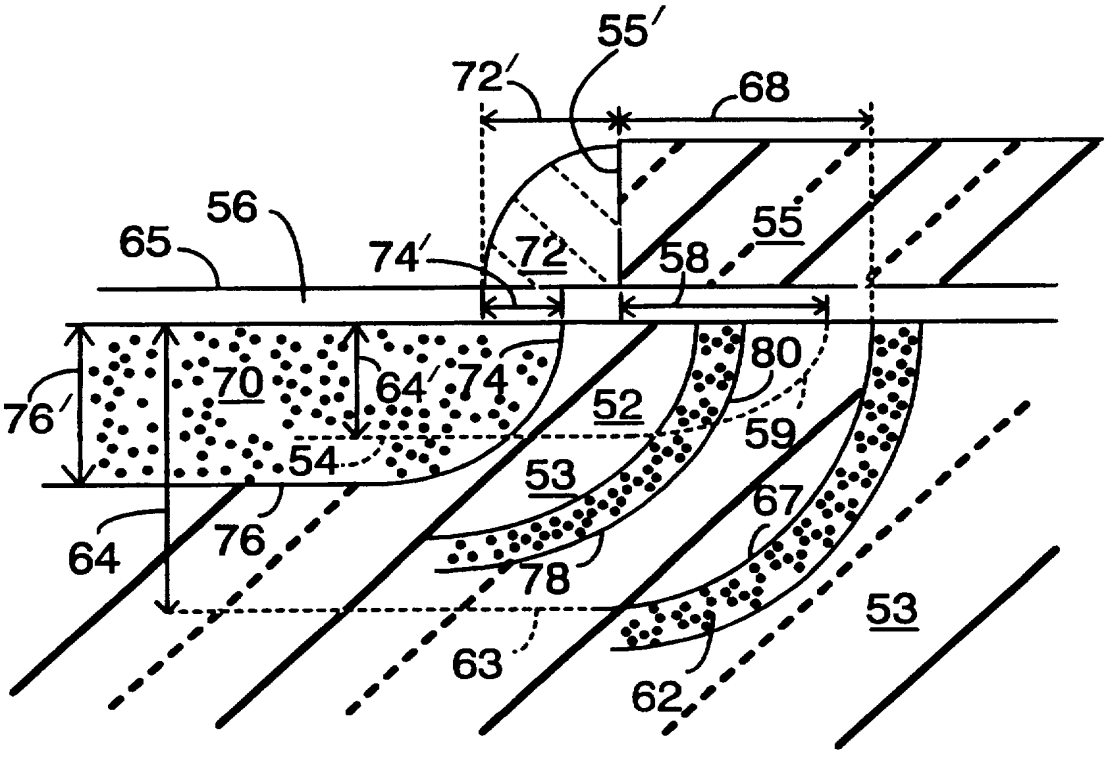
55′
72′
68
56
65
74′
72
58
55
70
64′
74
80
76′
52
59
54
53
67
64
76
78
53
63
62

FIG. 7

INTERNATIONAL SEARCH REPORT

ational Application No
PCT/US 97/05894

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/265 H01L21/336 H01L29/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 85 00694 A (KELLY M.J. ET AL) 14 February 1985	1-5,8,9
Y	see abstract	6,10
A	see page 3, line 17 - line 19 see page 4, line 31 - page 6, line 20 see page 3, line 29	7,11

Y	DE 42 13 244 A (MITSUBISHI ELECTRIC CORP) 29 October 1992 see abstract; figures 5-11	6,10

A	FR 2 578 096 A (BULL SA) 29 August 1986 see page 8, line 5 - line 10; figure 1 see abstract	1-10

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

3

Date of the actual completion of the international search	Date of mailing of the international search report
22 August 1997	04 -09- 1997

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Gélébart, J

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/05894

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 205 (E-420), 17 July 1986 -& JP 61 047670 A (TOSHIBA CORP), 8 March 1986, see abstract; figure 1	1,2,4-8, 10
A	MARCHETAUX J C ET AL: "Suppression of the lateral diffusion under the gate of an MOS transistor by argon implantation" IEEE TRANSACTIONS ON ELECTRON DEVICES, NOV. 1986, USA, vol. ED-32, no. 11, ISSN 0018-9383, pages 2508-2510, XP002038103 see the whole document	1-10
A	SANDERS I R ET AL: "The effect of argon implantation on the conductivity of boron implanted silicon" SOLID-STATE ELECTRONICS, AUG. 1977, UK, vol. 20, no. 8, ISSN 0038-1101, pages 703-707, XP002038108 see abstract	1
A	MILGRAM A ET AL: "Effect of argon implantation on the activation of boron implanted in silicon" APPLIED PHYSICS LETTERS, 15 MAY 1983, USA, vol. 42, no. 10, ISSN 0003-6951, pages 878-880, XP002038104 cited in the application see abstract	1
P,A	US 5 585 286 A (ARONOWITZ SHELDON ET AL) 17 December 1996 see abstract	1

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INTERNATIONAL SEARCH REPORT

National Application No
PCT/US 97/05894

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WO 8500694 A	14-02-85	CA 1222835 A	09-06-87
		EP 0151585 A	21-08-85
		JP 60501927 T	07-11-85
DE 4213244 A	29-10-92	JP 5136404 A	01-06-93
		US 5245208 A	14-09-93
FR 2578096 A	29-08-86	NONE	
US 5585286 A	17-12-96	NONE	